CHEMISTRY OF MATERIALS
Article

Chem. Mater. **2010,** *22,* 5377–5382 5377
DOI:10.1021/cm1018234

Polymer Brush As a Facile Dielectric Surface Treatment for High-Performance, Stable, Soluble Acene-Based Transistors

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Received June 30, 2010. Revised Manuscript Received August 13, 2010

We developed a facile dielectric surface modification using "grafting to" polymer brushes for high-performance and stable TES-ADT FETs. Polymer brushes were grafted onto oxide substrates by spin-coating and thermal annealing. TES-ADT FETs fabricated on top of the polymer brush layer showed excellent device performance—a field-effect mobility of 0.84 $cm^2/(V\ s)$ and an on/off current ratio of 1×10^6—that was superior to that of devices using conventional dielectric surface treatments such as HMDS and ODTS. During solvent annealing of the TES-ADT films, the mobile chains of the polymer brushes appear to profoundly influence the diffusion and crystallization of the TES-ADT molecules, while maximizing the $\pi-\pi$ interactions along the in-plane direction. Moreover, the polymer brushes yielded excellent electrical and environmental stability because of the complete surface coverage with minimal pinholes and defects.

1. Introduction

Organic field-effect transistors (OFETs) have recently attracted significant attention because of their use in flexible large-area active display backplanes.[1] OFET performance is dramatically influenced by the surface characteristics of the gate dielectric component layer because charge carrier transport in OFETs takes place within organic semiconductor monolayers near the dielectric interface.[2] The surface characteristics of the dielectric can determine the molecular ordering and film morphology of the organic semiconductor layers and the charge-trapping states at the interface.[2,3] Therefore, control over the semiconductor/dielectric interface can efficiently increase field-effect mobility of OFETs.

Self-assembled monolayers (SAMs) with various terminal functionalities and chain lengths have been widely used to control the semiconductor/dielectric interface.[1d,4] Oxide dielectrics treated with octadecyltrichlorosilane (ODTS) or hexamethyldisilazane (HMDS) show dramatically improved field-effect mobilities and lower off currents for a variety of semiconductors.[1d,4b−d] However, insufficient coverage or local structural defects in the SAMs, formed when condensation between SAM molecules and the oxide insulator substrate is incomplete, cannot be excluded. These features induce unfavorable crystalline order in the contacting semiconductor layer and produce charge trapping sites at the semiconductor/dielectric interface. Another dielectric surface modification technique is the insertion of a polymeric buffer layer, such as polystyrene (PS), polyvinyl phenol (PVP), or polyimide (PI).[5] In contrast with SAM functionalization, polymeric buffer layers involve a simple film deposition

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process, and surface coverage is relatively complete with minimal pinhole and defects. In addition, the chemical properties of the dielectric surface may be finely controlled via choice of the polymer. However, spin-coated polymeric buffer layer cannot be applied to the solution processable organic semiconductors because of the delamination of buffer layer during deposition of the organic semiconductor through the spin- or drop-casting.

An alternative strategy combines the advantages of both SAMs and polymeric buffer layers; specifically, polymer brushes that are tethered by one end to the substrate can be applied as dielectric surface chemical modifications. Compared to spin-coating of the polymeric buffer layer, polymer brushes produce covalently linked and strongly adherent polymeric layers, which can be applied to solution-processable organic semiconductors because they are impervious to delamination or cracking during solution processing. Moreover, the covalent bond formed between the surface and the polymer chain renders the polymer brush surface resilient to common chemical conditions. Tethering is sufficiently dense and the polymer chains are crowded, so the polymers form a densely packed pinhole-free film. However, in conventional "grafting from" methods for tethering polymers, the initiators should be immobilized onto the surface, followed by in situ surface-initiated polymerization such as cationic, anionic, or atom transfer radical polymerization (ATRP), which is high-cost, time-consuming, and poor throughput.[6]

Here, we present a new method for facile dielectric surface modification using an end-functionalized polymer to produce high-performance soluble acene FETs. Hydroxyl-functionalized polystyrene (PS) was grafted onto the oxide substrate by spin-coating and thermal annealing, resulting in a densely packed pinhole-free PS brush layer. Triethylsilylethynyl anthradithiophene (TES-ADT) FETs fabricated on top of the PS brush showed dramatically improved device performance, specifically, a field-effect mobility of 0.84 $cm^2/(V\ s)$, on/off current ratio of 10^6, and threshold voltage of 1.4 V. Moreover, PS brushes with high grafting density resulted in excellent electrical and environmental stability because of complete surface coverage with minimal pinholes and defects. This is a significant improvement over conventional dielectric surface treatments such as octadecyltrichlorosilane (ODTS) and hexamethyldisilazane (HMDS). These improvements in the FET performance can be described in terms of the semiconductor crystalline structure and the activation energy for trap creation in the TES-ADT films, which were investigated, respectively, by synchrotron X-ray diffraction (XRD) and quantitative analysis of the threshold voltage stability.

2. Experimental Section

Materials and Device Fabrication. To fabricate the OFETs, a highly doped n-type Si wafer with a thermally grown 300 nm thick oxide layer was used as the substrate. The wafer served as the gate electrode, whereas the oxide layer acted as a gate insulator. Prior to treating the silicon oxide surface, the wafer was cleaned in piranha solution for 30 min at 100 °C and washed with copious amounts of distilled water. Hydroxyl end-functionalized polystyrene (PS) with a molecular weight of M_n = 1.6 and 19.5 kg/mol (Polymer Source Inc.) was spin-coated onto the SiO_2 substrate from a 0.5 wt % toluene solution then heated at 170 °C for 48 h under a vacuum. Heating allowed the hydroxyl end group of the PS chains to react with the oxide layer in the SiO_2 substrate. The tethered PS brush modified substrate was rinsed with toluene to remove unreacted PS chains. Samples were annealed at 100 °C for 24 h in the vacuum chamber.[7] For comparison, octadecyltrichlorosilane (ODTS, Gelest, Inc.) and hexamethyldisilazane (HMDS, Aldrich Chemical Co.) were applied by a previously reported method. All samples on SiO_2 gate dielectrics were characterized by X-ray reflectivity, Fourier-transform infrared spectroscopy (FT-IR), atomic force microscopy (AFM), and contact angle measurements. 100 nm thick TES-ADT films were spin-coated from a 1.5 wt % hexane solution onto PS brush-treated substrates. TES-ADT films were solvent-vapor annealed for 30 min in a glass chamber using 1,2-dichloroethane vapor at a pressure of 10 kPa. After solvent annealing, the samples were dried in a vacuum chamber for 24 h. The devices were completed by evaporating Au through a shadow mask to define the source and drain contact electrodes on the TES-ADT film, with channel lengths and widths of 100 and 800 μm, respectively.

Characterization. The crystalline structure of the TES-ADT films was characterized by synchrotron X-ray diffraction (XRD) studies at the 5A beamline of the Pohang Accelerator Laboratory (PAL), Korea. Transistor current−voltage characteristics were measured using Keithley 2400 and 236 source/measure units at room temperature under ambient conditions in a dark environment.

3. Results and Discussion

TES-ADT FETs were built on heavily doped n-type Si substrates, which are commonly employed gate electrodes. A thermally grown 300 nm thick SiO_2 layer served as the gate dielectric. A simple "grafting to" method was used to graft hydroxyl-terminated polystyrene (PS−OH) onto the SiO_2 dielectric surface.[7] PS chains were anchored onto the SiO_2 by spin-coating PS−OH from a toluene solution followed by thermal annealing above the glass transition temperature of the PS, as shown in Figure 1a. The end-hydroxyl groups of PS−OH diffused to and reacted with SiO_2 by the condensation reaction between silanol groups on SiO_2 and PS−OH, thereby producing PS brushes on the substrate. To remove unreacted PS chains, the tethered PS brush modified substrate was rinsed with copious amount of toluene. The thickness of the PS brushes and the grafting density were controlled by the molecular weight of the PS−OH. In this study, two PS brushes with different molecular weights, M_n = 1.6 and 19.5k (hereafter referred to as *b*-PS1.6k and *b*-PS19.5k) were prepared. 100 nm thick TES-ADT films were spin-coated from a 1.5 wt % hexane solution onto the PS brush-treated substrates. Subsequently, TES-ADT films were solvent-vapor annealed for 30 min in a glass chamber with 1,2-dichloroethane vapor at

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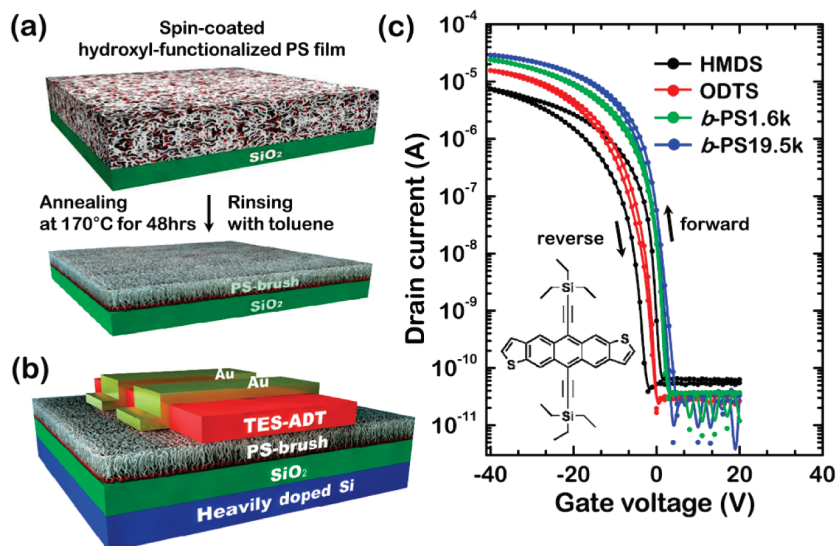

Figure 1. (a) Schematic representation of the PS brush formation via the "grafting to" method and (b) TES-ADT FETs based on the PS brush. (c) Transfer characteristics (I_D vs V_G) of TES-ADT FETs based on HMDS, ODTS, *b*-PS1.6k, and *b*-PS19.5k. the inset shows the chemical structure of TES-ADT.

Table 1. Surface Characteristics of HMDS, ODTS, and PS Brush-Treated SiO_2 Dielectrics, and the Electrical Properties of the OFET Devices

	dielectric surface properties			OFET properties		
dielectric surface modification	thickness (nm)	surface roughness (nm)	surface energy (mJ/m^2)	field-effect mobility (cm^2/(V s))	ON/OFF current ratio	V_{th} (V)
HMDS	0.52 (±0.03)	0.21 (±0.03)	43.6 (±1.2)	0.16 (±0.11)	1.3×10^5	0.4 (±1.9)
ODTS	1.72 (±0.05)	0.27 (±0.05)	25.6 (±2.3)	0.41 (±0.04)	4.9×10^5	−3.7 (±1.7)
b-PS1.6k	3.22 (±0.15)	0.21 (±0.04)	40.1 (±3.5)	0.64 (±0.09)	8.3×10^5	1.5 (±1.3)
b-PS19.5k	11.56 (±0.21)	0.28 (±0.03)	39.4 (±1.8)	0.84 (±0.16)	8.2×10^5	1.4 (±2.8)

a pressure of 10 kPa.[8] After solvent annealing, the samples were dried under vacuum for 24 h. The 50 nm Au source/drain electrodes were thermally evaporated through shadow masks. The channel lengths and widths were 100 and 800 μm, respectively. Figure 1b shows a schematic illustration of the top-contact TES-ADT FETs based on the PS brushes. For the comparison with conventional dielectric surface treatments, devices were also fabricated on HMDS- and ODTS-treated SiO_2 gate dielectrics. The quality of the HMDS and ODTS surfaces was confirmed by ellipsometry, atomic force microscopy (AFM), Fourier transform infrared spectroscopy (FT-IR), and X-ray reflectivity measurements. Figures S1 and S2 in the Supporting Information show the AFM images and X-ray reflectivity pattern of all samples, respectively. The dielectric surface properties are summarized in Table 1. Device performance was characterized by measuring the transfer characteristics and electrical/environmental stabilities.

Figure 1c shows the transfer characteristics (drain current (I_D)−gate voltage (V_G)) of TES-ADT FETs based on HMDS, ODTS, *b*-PS1.6k, and *b*-PS19.5k. The device performances of each FET, calculated in the saturation regime (V_D = −40 V), are summarized in Table 1. The capacitance values of the four gate dielectrics were similar to that of a 300 nm thick SiO_2 dielectric (∼11 nF/cm^2). The TES-ADT FETs fabricated on HMDS- and ODTS-treated SiO_2 gate dielectrics showed carrier mobilities of 0.16 and 0.41 cm^2/(V s), respectively. In contrast, the dielectric surface treatment with the PS brush yielded TES-ADT FETs with remarkably higher carrier mobilities of 0.64 and 0.84 cm^2/(V s) for *b*-PS1.6k and *b*-PS19.5k, respectively. This difference was ascribed to the crystalline structure of the TES-ADT films and charge traps at the TES-ADT/gate dielectric interface, discussed below. Moreover, TES-ADT FETs based on ODTS and PS brushes exhibited negligible hysteresis between the forward and reverse traces, whereas HMDS devices showed undesirable hysteresis. Because hysteresis depends crucially on charge traps formed by hydroxyl groups present at the semiconductor/dielectric interface, hydroxyl groups on the SiO_2 surface may not have been efficiently passivated by HMDS treatment.[5a,9] Charge trapping at the interface also affects charge transport in the channel region, which is reflected in the carrier mobilities of the FET devices.

The crystalline structures of the semiconductor TES-ADT layers, which influence charge mobility, were characterized by synchrotron XRD measurements. Panels a and b in Figure 2 show, respectively, the XRD intensities measured along the surface normal direction and the 2D grazing incidence X-ray diffraction (2D GIXD) patterns.

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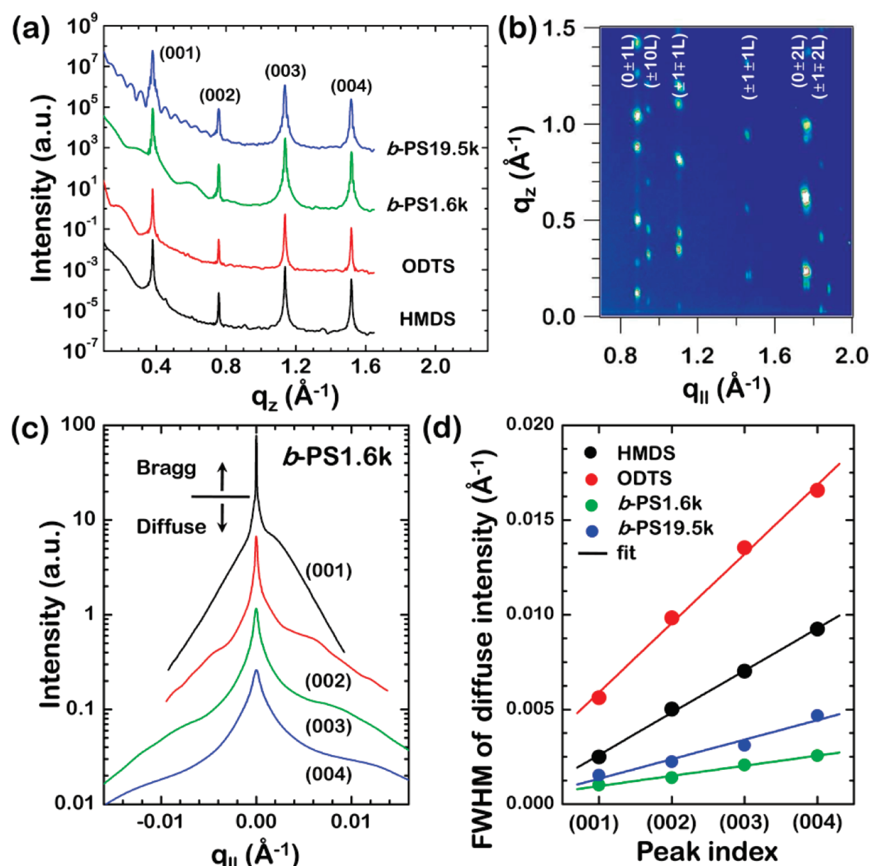

Figure 2. (a) X-ray intensities measured along surface normal direction of TES-ADT films that were solvent-annealed onto HMDS, ODTS, *b*-PS1.6k, and *b*-PS19.5k. (b) 2D GIXD patterns of TES-ADT films on *b*-PS1.6k. (c) Diffuse scattering intensities measured around the Bragg peaks of TES-ADT films on *b*-PS1.6k. The curves have been displaced vertically for clarity. (d) Plot of the fwhm of the diffuse intensity vs the peak index from the TES-ADT films.

The surface-normal diffraction patterns in Figure 2a consisted only of (00*l*) Bragg peaks, corresponding to a $d_{(001)}$-spacing of 1.66 nm between TES-ADT molecules, which indicates that the TES-ADT molecules stacked with the silyl groups oriented along the dielectric surface.[8b,10] The peak intensities that corresponded to the crystalline ordering along the surface normal direction did not differ between the samples. Moreover, the 2D GIXD patterns consisting of (*hkl*) Bragg peaks with nonzero in-plane indices *h* and *k*, as shown in Figure 2b, also exhibited similar crystallinities (see the Supporting Information for a discussion of the other samples).

Diffuse X-ray scattering intensities, observed around the Bragg peaks, revealed that samples with different surface treatments contained different crystalline disorder densities.[11] Diffuse scattering intensities were obtained from rocking sample scans around the Bragg peaks (Figure 2c); the incidence angle of the sample was varied at a fixed detector angle. In reciprocal space, this scan corresponds to a transverse scan, in which the in-plane component of the momentum transfer, $q_{||}$, was varied while the surface normal component, q_z, remained fixed. Such a measurement is sensitive to the lateral distribution of the crystalline disorder, for example, misfits, dislocations, and defects.[11] Rocking scan intensities consist of a sharp resolution-limited Bragg peak and broad diffuse scattering, as shown in Figure 2c. The diffuse scattering intensities clearly differed between the samples (see the Supporting Information). Remarkably, the full width at half-maximum (fwhm) of the diffuse scattering intensities increased linearly with the Bragg peak index, as shown in Figure 2d. Linearly increasing FWHMs of the diffuse intensities may have resulted from the crystalline disorder associated with line dislocations. The slope of a linear plot of the diffuse intensity width versus Bragg peak index yields a rough estimation of the dislocation density per unit area of the channel region.[11a] The dislocation densities of TES-ADT molecules crystallized onto PS brushes were calculated to be 6.8 ($\pm$0.4) $\times$ 10^9 and 11.4 ($\pm$0.6) $\times$ 10^9 cm^{-2} for *b*-PS1.6k, and *b*-PS19.5k, respectively. These values were dramatically lower than those of ODTS and HMDS surfaces, which were calculated to be 44.0 ($\pm$2.0) $\times$ 10^9 and 23.6 ($\pm$0.4) $\times$ 10^9 cm^{-2}, respectively.

This improved crystalline structure of the TES-ADT layer on the PS brushes may have been assisted by movements in the PS chains grafted onto SiO_2 during solvent annealing. When TES-ADT films were exposed to 1,2-dichloroethane vapor, 1,2-dichloroethane permeated not only the TES-ADT films, but also the PS chains. This imparted mobility to the TES-ADT molecules, which

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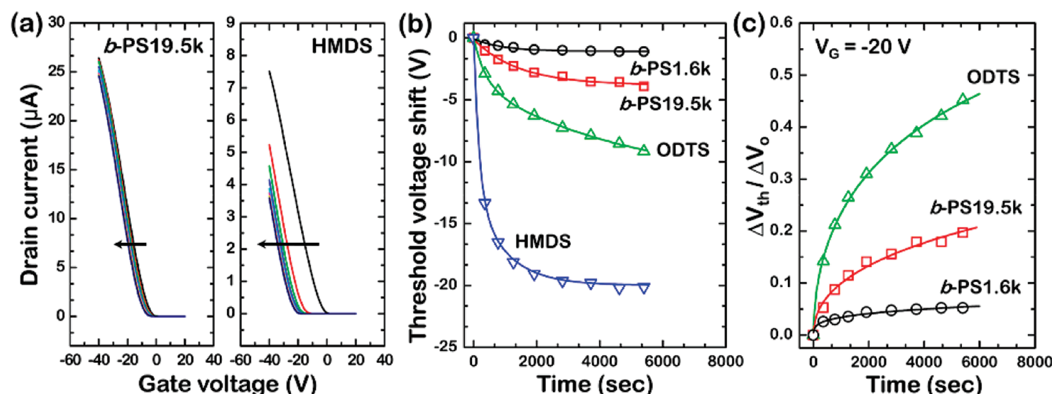

Figure 3. (a) Evolution of the linear transfer curves of TES-ADT FETs fabricated with *b*-PS19.5k and HMDS surfaces, as a function of bias stress time (0−90 min). The gate bias during stress was −20 V. (b) Relative threshold voltage shift (ΔV_{th}) of TES-ADT FETs as a function of stress time. (c) Plot of $\Delta V_{th}/V_o$ vs bias stress time for the TES-ADT FETs based on ODTS, *b*-PS1.6k, and *b*-PS19.5k. The solid curves were fit to a stretched exponential equation.

allows their structure to an energetically stable crystalline state. The mobility of PS chains during solvent vapor annealing, in contrast with the immobile HMDS and ODTS layers, may profoundly affect the movement and crystallization of TES-ADT molecules. This can maximize $\pi-\pi$ interactions along the in-plane direction, dramatically improving the carrier mobility of the device. Further investigations involving a variety of solution-processable organic semiconductors are underway to test this hypothesis. We note that this explanation may not be valid when interfacial charge trapping effects dominate. For example, the HMDS device characterized here showed considerable hysteresis in the transfer characteristics (Figure 1c) because of relatively higher charge traps, as discussed previously. This is the reason that the carrier mobility of HMDS devices is lower than that of ODTS devices although the dislocation density is lower than that of ODTS. Furthermore, we confirmed that the TES-ADT FETs fabricated on conventional, spin-coated PS layer did not show any transistor behavior because the PS layer might be further delaminated during solvent-vapor annealing.

Figure 3 show the electrical stabilities of TES-ADT FETs obtained by measuring the threshold voltage (V_{th}) as function of time under bias stress.[12a] A sustained gate bias (V_G) of −20 V was applied under ambient conditions over 90 min. Remarkably, the V_{th} shift was much smaller in the *b*-PS19.5k devices than in the HMDS devices, as shown in Figure 3a. The V_{th} shift is indicative of charge trapping instabilities in transistors.[12] The relative threshold voltage shifts (ΔV_{th}) of TES-ADT FETs fabricated using various surface treatments are summarized in Figure 3b. Compared with HMDS and ODTS devices, the magnitude of ΔV_{th} dramatically decreased for both devices based on PS brushes. Interestingly, almost no ΔV_{th} was observed in TES-ADT FETs based on *b*-PS1.6k, even though a thicker *b*-PS19.5k layer (11.56 nm) would be expected to more efficiently cover and passivate the traps on the SiO_2 surface than would the thinner *b*-PS1.6k layer (3.22 nm). This unexpected result was attributed to the grafting density of the PS brush. The grafting density of the polymer brush was calculated using $\sigma = \rho d_o N_A / M_n$, where d_o represents the brush height, the mass density of polymer is given by ρ ($\rho_{PS} = 1.05$ g/cm^3), and N_A and M_n represent Avogadro's number and the number average molecular weights of the polymer, respectively.[7] The grafting densities of *b*-PS1.6k and *b*-PS19.5k were calculated to be 1.27 and 0.37 chains/nm^2. Therefore, the *b*-PS1.6k treatment more efficiently covered the oxide surfaces, decreasing the charge trapping sites at the semiconductor/dielectric interface. On the other hand, ODTS devices showed a higher ΔV_{th}, although the grafting density of ODTS was much higher than that of the PS brushes. This was presumably due to local structural defects and grain boundaries induced by the crystalline nature of ODTS.[13] In the HMDS devices, HMDS formed a layer only a few angstroms thick that was insufficient to passivate traps on the SiO_2 surface. The ΔV_{th} for HMDS devices was as high as −20 V, as shown in Figure 3b.

The electrical stability of each TES-ADT FET was quantified by modeling the threshold voltage shift using the stretched exponential equation,[14]

$$\frac{V_{th} - V_{th,i}}{V_G - V_{th,i}} = 1 - \frac{1}{\{1 + \exp[(E_{th} - E_A)/k_B T_0]\}^{1/(\alpha - 1)}}$$

where $V_{th,i}$ is the initial V_{th}, E_A is the typical activation energy for trap creation, $k_B T_0$ is the slope of the activation energy distribution, and α is a constant. E_{th} corresponds to the thermalization energy, defined by $k_B T \ln(\nu t)$. Here, k_B and ν are the Boltzmann constant and attempt-to-escape frequency, respectively. The curves that described the dependence of the shift in V_{th} on the stress time were clearly fit by this equation, as shown in Figure 3c. This equation can be applied to OFETs with no hysteresis, such as the ODTS and PS brush devices. Here, the fitting parameters were E_A, $k_B T_0$, ν, and α. The optimal fit

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Table 2. E_A **and** k_BT **of TES-ADT FETs based on ODTS,** ***b*****-PS1.6k, and** ***b*****-PS19.5k-Treated Oxide Dielectrics**

	ODTS	*b*-PS1.6k	*b*-PS19.5k
E_A (meV)	57.2 (±0.4)	84.5 (±2.3)	63.8 (±0.8)
k_BT_0 (meV)	4.9 (±0.3)	9.1 (±0.6)	5.5 (±0.3)

yielded values for ν and α of 1×10^5 Hz and 1.5, respectively. These values agreed well with previously reported values.[14] The parameters associated with the activation energy, i.e., E_A and k_BT, varied with the surface treatment, as summarized in Table 2. The fits yielded E_A values of 57.2 (ODTS device), 84.5 (*b*-PS1.6k device), and 63.8 meV (*b*-PS19.5k devices). The negligible values of ΔV_{th} measured for TES-ADT FETs fabricated on *b*-PS1.6k, which showed a high grafting density, were attributed to higher activation energies for trap creation.[11b,14]

The long-term environmental stability of TES-ADT FETs stored in air in the dark for 4 months was examined, as shown in Figure 4. ODTS devices showed a huge reduction in on-current and a positive shift in the turn-on voltage after 4 months air storage. Hysteresis between the forward and reverse traces also dramatically increased. However, only slight degradation in the on-current and turn-on voltage was observed in the *b*-PS1.6k devices. The turn-on voltage shift, which is closely related to oxygen or impurity doping, was minimized when defect- and pinhole-free *b*-PS1.6k was applied to the SiO_2 substrate.[15] In contrast, the ODTS surface, which contained defects or grain boundaries, permitted the permeation of oxygen and other impurities into the interfaces. Because of the relatively complete passivation of SiO_2 by the PS brush, atmospheric oxygen or impurities barely permeated the semiconductor/dielectric interfaces, leading to a high environmental stability.

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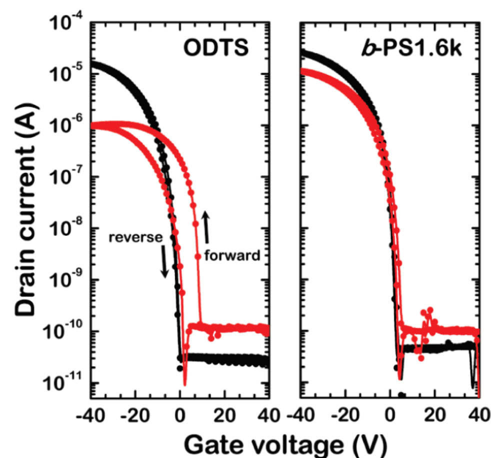

Figure 4. Long-term environmental stability of TES-ADT FETs fabricated with ODTS, and *b*-PS1.6k surfaces, stored in air in the dark for 4 months; black, as-prepared; red,: 4 months air storage.

4. Conclusions

In summary, a facile dielectric surface modification using the end-functionalized tethered polymer was developed for high performance soluble acene FETs. TES-ADT FETs fabricated on top of a PS brush showed dramatically improved device performance, specifically, a field-effect mobility of 0.84 $cm^2/(V\ s)$ and an on/off current ratio of 1×10^6. Moreover, the PS brush yielded excellent electrical and environmental stability due to the complete surface coverage with minimal pinholes and defects compared to conventional dielectric surface treatments.

Acknowledgment. This work was supported by the Korea Research Foundation Grant funded by the Korean Government (KRF-2008-313-C00231).

Supporting Information Available: Additional figures (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.